CLAIM LISTING

Please amend the claims as indicated below:

1. (Amended) A method for profiling the frequency that particular ones of a plurality of instructions are executed, said method comprising:

generating an interrupt;

storing an address from a program counter at the time of the interrupt;

generating a pseudo-random number after generating the interrupt;

loading a timer with a value that is a function of the pseudo-random number and a user provided parameter; and

updating a profile with the address from the program counter.

Claims 2 and 3 are cancelled without prejudice.

4. (Amended) The method of claim [2] 1, wherein the [psuedo] pseudo-random number is also a function of the address from the program counter.

5. (Original) The method of claim 1, wherein updating the profile further comprises: incrementing a count associated with an address range, the address range comprising the address in the program counter.

6. (Amended) An instruction memory storing a plurality of instructions, said plurality of instructions comprising:

a host operation for performing a host function, the host operation comprising a first plurality of instructions; and

an interrupt subroutine for interrupting the host function, said interrupt subroutine comprising:

a debugging tool for profiling the frequency that particular instructions of the first plurality of instructions are executed, wherein the debugging tool further comprises a second plurality of instructions, said second plurality of instructions further comprising:

updating a profile with the address in the program counter at the time of the interrupt;

generating a pseudo-random number after generating the interrupt; and

loading a timer with a value that is a function of the pseudo-random number and a user-provided parameter.

Claims 7 and 8 are cancelled without prejudice.

9. (Amended) The instruction memory of claim 7, wherein the [psuedo] pseudo-random number is also a function of the address from the program counter.

10. (Amended) An integrated circuit for performing a host function, said integrated circuit comprising:

a first memory for storing a host operation comprising a first plurality of instructions, a processor for executing the first plurality of instructions; a timer for interrupting the processor; and

a second memory for storing an interrupt subroutine, the processor executing the interrupt subroutine after the timer interrupts the processor; and

the interrupt subroutine comprising:

a debugging tool for measuring the frequency that particular instructions of the plurality of instructions are executed, wherein the debugging tool further comprises a second plurality of instructions, the second plurality of instructions comprising:

updating a profile with the address in the program counter at the time of the interrupt;

generating a pseudo-random number after generating the interrupt; and

loading a timer with a value that is a function of the pseudo-random number and a user-provided parameter.

13. (Original) The integrated circuit of claim 12, wherein updating the profile further comprises:

incrementing a count associated with an address range, the address range comprising the address in the program counter.

Claim 14 is cancelled without prejudice.

15. (Amended) The integrated circuit of claim 12, wherein the [pseudo] pseudo-random number is also a function of the address from the program counter.